PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number (Optional) 058268.00136
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]	Application Number: 09/492,265
	Filed: January 27, 2000
on _____	First Named Inventor: Yi-Hsien HAO et al.
Signature _____	Art Unit: 2616
Typed or printed Name _____	Examiner: Ng, Christine Y.

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a Notice of Appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
    Note: No more than five (5) pages may be provided.

I am the

☐   Applicant/Inventor.

☐   assignee of record of the entire interest.
      See 37 CFR 3.71. Statement under
      37 CFR 3.73(b) is enclosed

☒   Attorney or agent of record.
      Registration No._____51,091

☐   Attorney or agent acting under 37 CFR 1.34.
      Reg. No. is acting under 37 CFR 1.34 _____

_____
Signature

_____
David E. Brown
Typed or printed name

(703) 720-7800
Telephone number

December 20, 2007
Date

NOTE: Signatures of all of the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐   *Total of _____ forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Confirmation No.: 9668

Yi-Hsien HAO et al.   Art Unit: 2616

Application No.: 09/492,265   Examiner: Ng, Christine Y.

Filed: January 27, 2000   Attorney Dkt. No.: 58268.00136

For: MEMORY STRUCTURE FOR RESOLVING ADDRESSES IN A PACKET-BASED NETWORK SWITCH

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450   December 20, 2007

Sir:

In accordance with the Pre-Appeal Brief Conference Pilot Program guidelines set forth in the July 12, 2005 Official Gazette Notice, Applicants hereby submit this Pre-Appeal Brief Request for Review of the final rejections of claims 1-60 in the above identified application. Claims 1-60 were finally rejected in the Office Action dated August 20, 2007. Applicants filed a Response to the Final Office Action on October 22, 2007, and the Office issued an Advisory Action dated November 20, 2007 maintaining the final rejections of claims 1-60. Applicants hereby appeal these rejections and submit this Pre-Appeal Brief Request for Review.

The Office Action rejected claims 1-60 under 35 U.S.C. 103(a) as being obvious over US Patent No. 6,021,132 to Muller et al. (Muller), in view of US Patent No. 6,529,519 to Steiner et al. (Steiner), in further view of US Patent No. 6,427,185 to Ryals et al. (Ryals). The Office Action took the position that Muller disclosed all of the features of these claims except a single buffer per packet mechanism or an index key. The Office Action asserted that Steiner and Ryals disclosed these features respectively. Applicants submit that the cited references taken individually or in combination, fail to disclose or suggest all of the features of any of the pending claims. This failure constitutes clear error in the Office Action.

Claim 1, from which claims 2-7 depend, is directed to a memory structure. An Address Resolution Table resolves addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address. A Packet Storage Table, is adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claim 8, from which claims 9-12 depend, is directed to a memory structure. An Address Resolution Table having an associative memory structure uses a key to index a location within the Address Resolution Table. The Address Resolution Table resolves addresses in a packet-based network switch. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The key is a predefined portion of a packet destination address.

Claim 13, from which claims 14-27 depend, is directed to a memory structure having a memory block. The memory structure includes an Address Resolution Table having an associative memory structure. The Address Resolution Table resolves addresses in a packet-based network switch and using a key to index a location within the Address Resolution Table. A Transmit Descriptor Table is associated with a corresponding packet-based network transmit port, and the Transmit Descriptor Table is adapted to receive a Table Descriptor Address and a Table Descriptor Value. The Packet Storage Table is adapted to receive at least one of each of a Packet Data Address portion and a Packet Data Value portion. The memory structure also includes a single buffer per packet mechanism configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key wherein the key is a predefined portion of a packet destination address.

Claim 28, from which claims 29-31 depend, is directed to a packet-based switch. The packet-based switch includes a shared memory structure having an Address Resolution Table

and a Packet Storage Table. A key indexes a location within the Address Resolution Table wherein the key is a predefined portion of a packet destination address. A single buffer per packet mechanism is configured to receive an individual packet for enabling only one transmit descriptor read per the individual packet and for enabling an execution of a single access in order to locate an entire packet at the location using the key. The entire packet is to be transmitted.

Claims 32, 52, and 57 are also independent claims that are drawn to separate embodiments of the present invention.

Applicants respectfully submit that each of the above claims recites features that are neither disclosed nor suggested in the cited references.

As discussed in Applicants' previous correspondence, Muller is directed to shared memory management in a switch network element. Muller describes a shared memory manager 220 that is exploited by input and output ports 206 by locally storing pointers to buffers that contain packet data rather than locally storing the packet data. A predetermined number of buffer pointers are kept on hand to allow immediate storage of received packet data. The buffer pointers are preallocated during the initialization of switching element 100 and requested from shared memory manager 220. Pointers are queued to buffers that contain packet data, and not to the packet data itself. Further, a packet can be stored over more than one buffer. Each buffer in shared memory 230 is owned by one or more different ports at different points in time without having to duplicate the packet data.

As previously discussed, Steiner is directed to prioritized-buffer management for fixed size packets in a multimedia application. Steiner describes a memory system that includes a tag register for storing tags associated with respective pages, wherein each tag indicates whether the associated page is empty or full. A processor maintains a table of pointers to each packet boundary, and, therefore, knows the location of all leftover packets. A tag register 40 is provided, that has as many bits as there are packet boundaries of buffer 22.

Ryals is directed to a switching device includes network interface cards connected to a common backplane. Each interface card is configured to support the maximum transfer rate of the backplane by maintaining a "pending" queue to track data that has been received but for which the appropriate routing destination has not yet been determined. The switching device includes a switch controller that maintains a central card/port-to-address table. When an interface

card receives data with a destination address that is not known to the interface card, the interface card performs a direct memory access over a bus that is separate from the backplane to read routing data directly from the central table in the switch controller.

Applicants respectfully submit that the cited references fail to disclose or suggest all of the features of the above claims for the reasons set forth below.

Specifically, the cited combination of references fail to disclose or suggest at least the feature of "a Packet Storage Table, the Packet Storage Table adapted to receive a packet for storage in the packet-based network switch, and sharing a preselected portion of memory with the Address Resolution Table", as recited in claims 1, 8, 13, 28, 32, 52 and 57. The Office Action relied on Muller to disclose this feature. However, as admitted in the Office Action, and as discussed in Applicant's previous correspondence, Muller states that the Address Resolution Table (address table stored in forwarding memory 113), and the Packet Storage Table, (shared memory manager 220) do not <u>share a preselected portion of memory</u>, as recited in the presently pending claims. Applicants further submit that Steiner and Ryals fail to cure this deficiency.

The Advisory Action stated that the shared memory manager 220 and forwarding memory 113 are both part of the same subsystem 11, "thereby sharing the same memory." However, Applicants respectfully submit that the Advisory Action appears to be reading features into Muller that simply do not exist. Nowhere in Muller is it either disclosed or suggested that the shared memory manager 220 and forwarding memory <u>share a presented portion of memory</u>, as recited in the independent claims. This omission constitutes clear error in the Office Action..

To establish *prima facie* obviousness the prior art references must teach or suggest all the claim limitations. <u>In re Vaeck</u>, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). As discussed above, the Office Action failed to establish *prima facie* obviousness because they cited references fail to disclose or suggest all of the features recited in any of the pending claims. This failure constitutes clear error in the Office Action
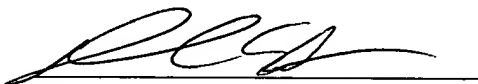
As also stated in Applicant's previous correspondence, in US Patent law a piecemeal analysis of a number of references, to extract a number of individual elements which are picked and chosen to recreate the claimed invention, is improper absent some teaching or suggestion in the references to support their use in the particular claimed combination. It is improper to use applicant's own disclosure for any such motivation or incentive.

As previously discussed, both Steiner ad Ryals are combined with Muller in a piecemeal manner to recreate the features recited in the presently pending claims. For example, Ryals is combined with Muller and Steiner to add the feature the key is a predefined portion of a packet destination address. One skilled in the art would not otherwise be motivated to combine Ryals with Muller and Steiner except for the benefit of recreating Applicant's invention.

Based at least on the above, Applicants respectfully submit that the cited references, taken individually or in combination, fail to disclose or suggest all of the features recited in claims 1-60. This failure constitutes clear error in the Office Action. Accordingly, withdrawal of the rejection under 35 U.S.C. 103(a) is respectfully requested.

Reconsideration and withdrawal of the rejections, in view of the clear errors in the Office Action, is respectfully requested. In the event this paper is not being timely filed, the applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,

David E. Brown
Registration No. 51,091

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800; Fax: 703-720-7802

DEB:jkm

Enclosures: PTO/SB/33 Form
              Notice of Appeal
              Petition for Extension of Time
              Check No. 017773